UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/903,828	07/11/2001	Hung Qui Le	AT9-98-038-US2	1565

7590 03/30/2005

Attention: Barry S. Newberger
Winstead Sechrest & Minick P.C.
5400 Renaissance Tower
1201 Elm Street
Dallas, TX 75270-2199

EXAMINER	
CHANG, JUNGWON	
ART UNIT	**PAPER NUMBER**
2154	

DATE MAILED: 03/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/903,828	LE ET AL.	
	Examiner	Art Unit	
	Jungwon Chang	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,10-17,19,25-34 and 38-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,10-17,19,25-34 and 38-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 7-9, 18, 20-24 and 35-37 are cancelled and claims 38-52 are added in preliminary amendment filed on 7/11/2001. Claims 1-6, 10-17, 19, 25-34 and 38-52 are presented for examination.

2. Claim 10 is objected to because of the following informalities:

Line 2, "includes a includes a" should be "includes a".

Appropriate correction is required.

3. The disclosure is objected to because reference character "164" has been used to designate both "target tag" and "source operand tag" (please see specification, page 2 – page 3, line 16); and reference character "166" has been used to designate both "source tag" and "target operand tag" (please see specification, page 2 – page 3, line 16). Appropriate correction is required.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA

1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1-6 and 10 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,308,260. Although the conflicting claims are not identical, they are not patentably distinct from each other because both apparatus claimed in instant application and the patent No. 6,308,260 comprise substantially the same elements.

Claim 1 of Pat. No. 6,308,260	Application claims 09/903,828
1. An apparatus of self-initiated instruction issuing comprising: an instruction queue operable for issuing at least one instruction to an execution unit, said queue including a plurality of entries, each queue entry having a first portion and a second portion, said first portion operable for storing storing a first link data value and said second portion For storing a first data value, and wherein said first data value in a first queue entry is set in response to a first link data value in a preselected second queue entry, and wherein at least one instruction is selected For issuing in response to a predetermined first data value in a corresponding queue entry;	1. An apparatus of self-initiated instruction issuing comprising: an instruction queue operable for issuing at least one instruction to an execution unit, said queue including A plurality of entries, each queue entry having a first portion and a second portion, said first portion operable for storin storing a first link data value and said second portion for storing a first data value, and wherein said first data value in a first queue entry is set in response To a first link data value in a preselected second queue entry, and wherein at least one instruction is selected for issuing in response to a predetermined first data value in a corresponding queue entry.

a rename register device coupled to said queue, said rename register device including a plurality of entries, each entry having a first portion operable for storing a pointer data value and a second portion operable for storing a validity data value, wherein each said pointer data value is associated with a corresponding queue entry, and wherein each said first link data value is set in response to said pointer data values and said validity data values,	2. The apparatus of claim 1 further comprising A rename register device coupled to said queue, said rename register device including a plurality of entries, each entry having a first portion operable for storing a pointer data value and a second portion operable for storing a validity data value, wherein each said pointer data value is associated with a corresponding queue entry, and wherein each said first link data value is set In response to said pointer data values and said validity data values.
wherein each said rename register device entry includes third portion operable for receiving a plurality of operand tags, and wherein each said pointer data value is operable for selection in response to a preselected one of said plurality of operand tags;	3. The apparatus of claim 1 further comprising wherein each said rename register device entry includes third portion operable for receiving a plurality of operand tags, and wherein each said pointer data value is operab for selection in response to a preselected one of said plurality of operand tags.
wherein each said queue entry includes a third portion coupled to said rename register device for receiving a first one of said plurality of operand tags, and a fourth portion coupled to said rename register device for receiving a second one of said plurality of operand tags, wherein said first and second operand tags are associated with a dispatching instruction, and wherein said first operand tag is further associated with said first link data value;	4. The apparatus of claim 3 further comprising wherein each said queue entry includes a third portion coupled to said rename register device for receiving a fir one of said plurality of operand tags, and a fourth portion coupled to said rename register device for receiving a second one of said plurality of operand tags, wherein sai first and second operand tags are associated with a dispatching instruction, and wherein said first operand tag is further associated with said first link data value.
wherein said queue is operable for broadcasting a preselected first operand tag;	5. The apparatus of claim 4 wherein said queue is opera for broadcasting a preselected first operand tag.
a storage device operable for receiving said broadcasting of said first operand tag; and	6. The apparatus of claim 5 further comprising a storage device operable for receiving said broadcasting of said first operand tag.
wherein said storage device is coupled to said rename register device, and wherein each said rename register device entry includes a fourth portion operable for storing a second data value; said second data value being operable for setting in response to said broadcast first operand tag.	10. The apparatus of claim 2 wherein each said rename register device entry includes a fourth portion operable fo storing a second data value, said second data value bein operable for setting in response to an issuing instruction.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-6, 10-17, 19, 25-34 and 38-52 are rejected under 35 U.S.C. 102(e) as being anticipated by Cheong et al. (US 5,913,048), hereinafter referred to as Cheong.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

8. As to claim 1, Cheong discloses the invention as claimed, including an apparatus for self-initiated instruction issuing comprising:

an instruction queue (instruction queue, 1219, fig. 12; col. 6, lines 64-67) operable for issuing at least one instruction to an execution unit (col. 7, lines 1-27; col. 10, lines 48-51; instruction is ready to be issued for execution; col. 11, lines 27-34), said queue including a plurality of entries (fig. 3), each queue entry having a first portion and

a second portion (fig. 3), said first portion operable for storing a first link data value (TID; 118, 128a, 128b, valid/tagged; 124a, 124b, fig. 3; col. 11, lines 39-45) and said second portion operable for storing a first data value (value; 126a, 126b, fig. 3; col. 11, lines 31-45), and wherein said first data value in a first queue entry is set in response to a first link data value in a preselected second queue entry (col. 11, lines 31-45), and wherein at least one instruction is selected for issuing in response to a predetermined first data value in a corresponding queue entry (col. 11, lines 4-20 and 39-45).

9. As to claim 2, Cheong discloses a rename register device (1233, 1237, fig. 12) coupled to said queue (1219, fig. 12), said rename register device including a plurality of entries (figs. 1-2; col. 9, lines 37-48), each entry having a first portion operable for storing a pointer data value (TID; 104; fig. 1) and a second portion operable for storing a validity data value (value; 102, fig. 1), wherein each said pointer data value is associated with a corresponding queue entry (col. 9, line 49 – col. 10, line 3), and wherein each said first link data value is set in response to said pointer data values and said validity data values (col. 10, lines 40-47).

10. As to claim 3, Cheong discloses each said rename register device entry (figs. 1-2; col. 9, lines 37-48) includes a third portion operable for receiving a plurality of operand tags (100, fig. 1; 112, fig. 2), and wherein each said pointer data value is operable for selection in response to a preselected one of said plurality of operand tags (col. 8, lines 26-36; col. 9, line 49 – col. 10, line 3).

11. As to claim 4, Cheong discloses each said queue entry includes a third portion coupled to said rename register device for receiving a first one of said plurality of operand tags, and a fourth portion coupled to said rename register device for receiving a second one of said plurality of operand tags (col. 11, lines 12-16), wherein said first and second operand tags are associated with a dispatching instruction, and wherein said first operand tag is further associated with said first link data value (col. 11, lines 12-21).

12. As to claim 5, Cheong discloses said queue is operable for broadcasting a preselected first operand tag (col. 11, lines 39-45).

13. As to claim 6, Cheong discloses a storage device operable for receiving said broadcasting of said first operand tag (col. 5, line 59 – col. 6, line 2; col. 6, lines 34-40 and 64-67; col. 12, lines 19-31).

14. As to claims 10 and 11, Cheong discloses each said rename register device entry includes a fourth portion operable for storing a second data value, said second data value being operable for setting in response to an issuing instruction (col. 9, lines 52-65; col. 12, line 66 – col. 13, line 10).

15. As to claim 12, it is rejected for the same reasons set forth in claims 1 and 4 above.

16. As to claim 13, Cheong discloses each said second link data value is set in response to said pointer data values and said validity data values (col. 13, lines 43-60; col. 14, lines 15-29).

17. As to claim 14, it is rejected for the same reasons set forth in claim 1 above. In addition, Cheong discloses selecting for issuing an instruction associated with said entry containing said predetermined data value in said first portion in response to said predetermined data value (col. 10, lines 48-51; instruction is ready to be issued for execution; col. 11, lines 27-34).

18. As to claims 15-17, 19 and 25, Cheong discloses if said dispatching instruction is a one-cycle piped instruction (dispatching one instruction per cycle; col. 12, lines 35-36), storing a first queue pointer data value associated with said dispatching instruction in a first portion of an associated rename register entry, said rename register including a plurality of entries, wherein said queue pointer value associates said rename register entry and said preselected queue entry corresponding to said dispatching instruction, and wherein said second queue entry is selected in response to a second queue pointer value (col. 11, lines 4-21; col. 14, lines 15-29; col. 16, lines 15-32).

19. As per claim 26, Cheong discloses said second queue pointer value corresponds to a queue entry of an instruction target operand tag matching said source operand (col.

13, line 43 – col. 14, line 29).

20. As per claim 27, Cheong discloses first data value comprising a link mask having a number of bits equal to a number of entries in said queue (fig. 5A; col. 13, lines 61-64).

21. As per claim 28, Cheong discloses the step of setting said predetermined data value is in response to an issuing of an instruction associated with said second queue entry (col. 11, lines 40-45).

22. As to claim 29, it is rejected for the same reasons set forth in claim 1 above. In addition, Cheong discloses an input means (1024, 1026, 1032, fig. 10) for communicating a plurality of instructions (col. 6, lines 5-17);
a dispatch unit (1220, fig. 12) coupled to said input means (col. 7, lines 50-51); and at least one execution unit (1222, 1228, 1230, fig. 12) coupled to said dispatch unit for receiving instructions communicated therefrom, each execution unit including a self-initiated instruction issue mechanism for receiving said instructions and issuing instructions to an execution logic circuit for execution (col. 7, lines 50-54).

23. As to claim 30, it is rejected for the same reasons set forth in claim 3 above.

24. As to claim 31, it is rejected for the same reasons set forth in claim 5 above.

25. As to claim 32, it is rejected for the same reasons set forth in claim 6 above.

26. As to claims 33 and 34, they are rejected for the same reasons set forth in claims 10 and 11 above.

27. As to claim 38, Cheong discloses an apparatus for self-initiated processor instruction issuing including an issue queue (1219, fig. 12; col. 6, lines 64-67), said issue queue comprising a plurality of entries (fig. 3), each entry of said plurality operable for containing information associated with an instruction to be issued (col. 10, lines 48-51; col. 11, lines 27-34), wherein each entry includes a first portion for storing an instruction operand (120, fig. 3; operational code of the instruction; col. 11, lines 6-8) and a second portion for storing a link value (valid/tag; 100, 118, 128a, 128b; fig. 3; col. 11, lines 4-21), and wherein, for an instruction corresponding to a first entry having a value of said instruction operand determined by an instruction corresponding to a second entry, said link value in said second entry comprises a value corresponding to a number of said first entry (the processing of one instruction depends on a result from another instruction; col. 2, lines 32-65; col. 9, lines 48-65; col. 15, lines 4-35).

28. As to claim 39, Cheong discloses for said first entry comprising an "*i*th" entry of said plurality of entries, said value representing said first entry is a value of an "*i*th" bit of a plurality of bits of said link value in said second entry (fig. 3; col. 10, line 66 – col. 11, line 21).

29. As to claims 40, 42 and 43, they are rejected for the same reasons set forth in claim 2 above.

30. As to claim 41, Cheong discloses a data value in said third portion is operable for signaling an operand in a second portion of a corresponding entry of said plurality of entries is ready (col. 11, lines 27-34; col. 20, line 49 – col. 21, line 22).

31. As to claim 44, Cheong discloses said instruction corresponding to said second entry comprises a one-cycle piped instruction (col. 12, lines 35-36).

32. As to claim 45, Cheong discloses setting a predetermined value (predicted value) in a first portion of an entry in an instruction queue corresponding to a first instruction in response to a dispatch of a second instruction (col. 15, lines 4-35; col. 20, lines 21-25 and 37-48); and writing said predetermined value in a second portion of an entry in said instruction queue corresponding to said second instruction in response to an issuing of said first instruction, wherein a target of said first instruction comprises a source operand of said second instruction (col. 17, lines 15-23; col. 19, lines 50-58).

33. As to claim 46, Cheong further discloses validity value stored in an entry in a rename unit (1233, fig. 12; col. 9, line 49 – col. 10, line 3) coupled to said instruction queue (1219, fig. 12) (col. 11, line 4-21).

34. As to claim 47, Cheong discloses said first instruction is a one-cycle piped instruction (col. 12, lines 35-36).

35. As to claim 48, it is rejected for the same reasons set forth in claims 1 and 29 above. In addition, Cheong discloses an instruction storage unit (instruction cache and MMU; 1214, fig. 12; col. 6, lines 46-67).

36. As to claim 49, it is rejected for the same reasons set forth in claim 39 above.

37. As to claim 50, it is rejected for the same reasons set forth in claim 2 above.

38. As to claim 51, it is rejected for the same reasons set forth in claim 3 above.

39. As to claim 52, Cheong discloses said instruction corresponding to said second entry comprises a one-cycle piped instruction (col. 12, lines 35-36).

Conclusion

40. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Quarnstrom et al, patent 5,875,340, Le et al, patent 6,308,260, Cheong et al, patent 5,974,524, Cheong et al, patent 5,887,161, Chiarot et al, patent 6,061,785, Eisen et al,

patent 6,098,168, Chanmdani et al, patent 6,112,019, Witt, patent 6,212,623, Eisen et al, patent 6,289,437 disclose method and system for dispatching an instruction and source information to a queue, determining validity of the source information and issuing the instruction for execution in response to the source information validity.

41. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jungwon Chang whose telephone number is 571-272-3960. The examiner can normally be reached on 9:30-6:00 (Monday-Friday).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John A Follansbee can be reached on 571-272-3964. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JWC
March 28, 2005